CLAIMS

What is claimed is:

1. A programmable logic device (PLD), comprising:

a non-homogeneous array of programmable logic blocks;

an array of standardized interconnect blocks, each interconnect block being coupled to other interconnect blocks adjacent thereto in the array; and

an array of standardized test structures, each test structure being coupled between one of the interconnect blocks and one of the logic blocks.

2. The PLD of Claim 1, wherein the non-homogeneous array of programmable logic blocks includes additional logic blocks coupled directly to the interconnect blocks, in addition to at least two different types of the logic blocks that are coupled to the standardized test structures.

3. The PLD of Claim 1, wherein the non-homogeneous array of programmable logic blocks includes at least two of the following types of logic blocks: configurable logic elements (CLEs), input/output blocks (IOBs), random access memory blocks (BRAMs), and digital clock manager blocks (DCMs).

4. The PLD of Claim 3, wherein the non-homogeneous array of programmable logic blocks includes a plurality of CLEs coupled directly to the interconnect blocks, in addition to at least two different types of the logic blocks that are coupled to the standardized test structures.

5. The PLD of Claim 1, wherein all of the standardized interconnect blocks are logically equivalent.

6. The PLD of Claim 1, wherein:

each logic block comprises an input terminal and an output terminal;

each standardized interconnect block comprises an output terminal coupled to the input terminal of an associated logic block and further comprises an input terminal; and

each standardized test structure comprises a first multiplexer (MUX) having input terminals coupled to the input and output terminals of an associated logic block, an output terminal coupled to the input terminal of an associated standardized interconnect block, and a select input terminal.

7. The PLD of Claim 6, wherein the select terminal of the multiplexer is coupled to a configuration memory cell.

8. The PLD of Claim 6, wherein each standardized test structure further comprises a plurality of additional MUXes coupled between input and output terminals of the associated logic block and input terminals of the associated standardized interconnect block, the plurality of additional MUXes each having a select input terminal coupled to the select input terminal of the first MUX in the same standardized test structure.

9. The PLD of Claim 8, wherein the select input terminals of the first MUX and the additional MUXes in each standardized test structure are each controlled independently of the other standardized test structures.

10. The PLD of Claim 9, wherein the select input terminals of the first MUX and the additional MUXes in each standardized test structure are controlled by a single configuration memory cell.

11. The PLD of Claim 6, wherein each standardized test structure further comprises a second MUX, the second MUX comprising:

a select input terminal;

an output terminal coupled to an input terminal of the first MUX;

a first input terminal coupled to the input terminal of the associated logic block; and

a second input terminal coupled to a second input terminal of the associated logic block and further coupled to a second output terminal of the associated standardized interconnect block.

12. The PLD of Claim 11, wherein each standardized test structure further comprises first and second configuration memory cells coupled to the select input terminals of the first and second MUXes, respectively.

13. The PLD of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

14. A method of testing programmable interconnect in a programmable logic device (PLD), the PLD comprising an array of standardized interconnect blocks coupled to one another, an array of standardized test structures each coupled to and associated with one of the interconnect blocks, and a non-homogeneous array of programmable logic blocks each coupled to and associated with at least one of the test structures, the method comprising:

configuring the PLD with a configuration containing signal paths that traverse the standardized interconnect blocks and the standardized test structures and bypass the logic blocks, the configuration being the same for each of the standardized interconnect blocks and standardized test structures associated with each of the logic blocks;

applying an input test signal to a start point of each of the signal paths; and

observing an output test signal at an end point of each of the signal paths.

15. The method of Claim 14, wherein the non-homogeneous array of programmable logic blocks includes additional logic blocks coupled directly to the interconnect blocks, and the method further comprises configuring the additional logic blocks to mimic behavior of the standardized test structures in a test mode.

16. The method of Claim 14, wherein the non-homogeneous array of programmable logic blocks includes at least two of the following types of logic blocks: configurable logic elements (CLEs), input/output blocks (IOBs), random access memory blocks (BRAMs), and digital clock manager blocks (DCMs).

17. The method of Claim 16, wherein the non-homogeneous array of programmable logic blocks includes CLEs coupled directly to the interconnect blocks, and the method further comprises configuring the CLEs to mimic behavior of the standardized test structures in a test mode.

18. The method of Claim 14, wherein configuring the PLD comprises configuring each test structure to select one of at least two output signals from an associated interconnect block to add to a signal path through the test structure.

19. The method of Claim 14, wherein the PLD is a field programmable gate array (FPGA).

20. A computer-readable storage medium comprising computer-executable code for testing programmable interconnect in a programmable logic device (PLD), the PLD comprising an array of standardized interconnect blocks coupled to one another, an array of standardized test structures each coupled to and associated with one of the interconnect blocks, and a non-homogeneous array of programmable logic blocks each coupled to and associated with at least one of the test structures, the medium comprising:

code for configuring the PLD with a configuration containing signal paths that traverse the standardized interconnect blocks and the standardized test structures and bypass the logic blocks, the configuration being the same for each of the standardized interconnect blocks and standardized test structures associated with each of the logic blocks;

code for applying an input test signal to a start point of each of the signal paths; and

code for observing an output test signal at an end point of each of the signal paths.

21. The computer-readable storage medium of Claim 20, wherein the non-homogeneous array of programmable logic blocks includes additional logic blocks coupled directly to the interconnect blocks, and the storage medium further comprises code for configuring the additional logic blocks to mimic behavior of the standardized test structures in a test mode.

22. The computer-readable storage medium of Claim 20, wherein the non-homogeneous array of programmable logic blocks includes at least two of the following types of logic blocks: configurable logic elements (CLEs), input/output blocks (IOBs), random access memory blocks (BRAMs), and digital clock manager blocks (DCMs).

23. The computer-readable storage medium of Claim 22, wherein the non-homogeneous array of programmable logic blocks includes CLEs coupled directly to the interconnect blocks, and the storage medium further comprises code for configuring the CLEs to mimic behavior of the standardized test structures in a test mode.

24. The computer-readable storage medium of Claim 20, wherein the code for configuring the PLD comprises code for configuring each test structure to select one of at least two output signals from an associated interconnect block to add to a signal path through the test structure.

25. The computer-readable storage medium of Claim 20, wherein the PLD is a field programmable gate array (FPGA).

26. A system for testing programmable interconnect in a programmable logic device (PLD), the PLD comprising an array of standardized interconnect blocks coupled to one another, an array of standardized test structures each coupled to and associated with one of the interconnect blocks, and a non-homogeneous array of programmable logic blocks each coupled to and associated with at least one of the test structures, the system comprising:

a configuration module for configuring the PLD with a configuration containing signal paths that traverse the standardized interconnect blocks and the standardized test structures and bypass the logic blocks, the configuration being the same for each of the standardized interconnect blocks and standardized test structures associated with each of the logic blocks;

a test input module for applying an input test signal to a start point of each of the signal paths; and

a test observation module for observing an output test signal at an end point of each of the signal paths.

27. The system of Claim 26, wherein the non-homogeneous array of programmable logic blocks includes additional logic blocks coupled directly to the interconnect blocks, and the system further comprises an additional configuration module that configures the additional logic blocks to mimic behavior of the standardized test structures in a test mode.

28. The system of Claim 26, wherein the non-homogeneous array of programmable logic blocks includes at least two of the following types of logic blocks: configurable logic elements (CLEs), input/output blocks (IOBs), random access memory blocks (BRAMs), and digital clock manager blocks (DCMs).

29. The system of Claim 28, wherein the non-homogeneous array of programmable logic blocks includes CLEs coupled directly to the interconnect blocks, and the system further comprises an additional configuration module that configures the CLEs to mimic behavior of the standardized test structures in a test mode.

30. The system of Claim 26, wherein the configuration module configures each test structure to select one of at least two output signals from an associated interconnect block to add to a signal path through the test structure.

31. The system of Claim 26, wherein the PLD is a field programmable gate array (FPGA).